REMARKS

Claim 54 is added. Claims 24-31, 36, 37, 39-41 and 45-54 are in the application for consideration.

The specification is objected to under 35 USC §132 for the undersigned's alleged introduction of new matter by the last-filed amendment. Further, claims 36, 37, 40 and 41 are rejected under 35 USC §112, first paragraph for the undersigned's claiming in the last-filed amendment of the alleged specification new matter. The Examiner alleges that, with respect to the recited insulative cap, new matter is "clearly" introduced into the specification. The undersigned strongly disagrees with the Examiner's assertions.

The Examiner is reminded that this application as-filed included a specification, drawings and claims. It is axiomatic that all of these originally filed components constitute the as-filed application upon which any later amendment must be analyzed for the consideration of whether new matter has been added. The undersigned believes the Examiner has overlooked where Applicant pointed out in its last-filed response that the material added by amendment was not "new matter". Specifically, support for that which Applicant added in the last-filed amendment for both the specification and the claims can be found in Figs. 7-9 and in the specification as filed at p.9, lns.13-16. Even more specifically, the Examiner's attention is directed to p.9, ln.16, the fourth, fifth and sixth words, which cite "an insulative cap".

Accordingly, there clearly is support in Applicant's specification as filed for the now recited "an insulative cap". Further in addition to the specification disclosure, the depicted Figs. 7-9 illustrate such insulative cap.

Even ignoring the Examiner's mistaken assertion that the specification does not support the inserted language, clearly the outer caps of the illustrated line of floating gates 12 and 14 must be insulative. Specifically, the conductive materials 38, 9 of conductive line 40 in Fig. 7 are clearly shown as being in physical contact with the outer caps of lines of floating gates 12 and 14. The outer caps thereof must be insulative, or a fatal source to control gate short would occur in the depicted embodiment. Would the Examiner assert that the disclosed invention constitute inoperable circuitry? The answer is self-evident that Applicant clearly discloses operative circuitry, and that the outer cap must be insulative, even not withstanding Applicant's inherent disclosure of same in its application as filed at p.9, ln.16.

Applicant's exemplary physical structures, at least as shown in Fig. 7 as-filed, depict sidewall spacers 42 having uppermost/outermost surfaces which are elevationally coincident with the outer surface of the illustrated insulative caps. Accordingly, Applicant's drawings as-filed inherently disclose that which Applicant recites in the rejected claims 36 and 37. The specification is amended at p.13 and p.15 to recite this inherently disclosed subject matter of the drawings as-filed, and to provide specification language support for that which is recited in claims 36 and 37. Accordingly, no new matter is added

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thereby. The subject paragraph on p.9, starting at ln.4 is also amended to provide the reader with an inherent description to that which Applicant shows in its drawings, and which is clearly supported from the as-filed documents. Again, no new matter is added thereby for the reasons argued above.

The undersigned feels he has gone to great lengths in this Response to clearly point out to the Examiner where in the specification and drawings there is support for the added clarifying language in the specification and claims. Accordingly, it is respectfully requested that the Examiner withdraw the new matter and §112, first paragraph, rejections. If the Examiner is to persist in this regard, it is specifically requested that the Examiner point out how the subject matter is new matter, rather than merely pointing to the objected to language and stating that such is "clearly" not supported. In such event, a quick telephone interview is requested to facilitate the prosecution and ultimate conclusion of this issue. The Examiner's consideration in this regard would be sincerely appreciated.

New claim 54 is added. Support for the same is inherent in Applicant's application as filed at p.8, ln.9. Accordingly, no new matter is added thereby.

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This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 4-30-02

By: _____
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/768,878
Filing Date . . . . . January 23, 2001
Inventor . . . . . Graham Wolstenholme
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2812
Examiner . . . . . Richard A. Booth
Attorney's Docket No. MI55-003
Title: Methods of Forming a Line of FLASH Memory Cells

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO MARCH 29, 2002 FINAL OFFICE ACTION

In the Specification

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

The paragraph beginning at line 4 on page 9 has been amended as follows:

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Fig. 2 illustrates trenches 16 having been filled with an insulating dielectric material 20, such as high density plasma deposited oxide, and subjected to a planarization step to provide a substantially planar outer surface. At this point in the process, such effectively forms an alternating series of trench isolation regions 22 and active area regions 18 in semiconductor substrate 11 running in a line adjacent and along lines of floating gates 12 and 14. The semiconductor wafer is typically and preferably fabricated to a point as would be depicted in Fig. 2, with the lines of floating gates being fabricated thereafter. Lines of floating gates 12 and 14 preferably constitute a gate dielectric layer (not shown), floating gate regions 23 (Fig. 1), an interpoly dielectric layer (not shown), a conductively doped polysilicon/silicide stack (not shown), and an insulative cap (not shown). (Such "not shown" items of this first described embodiments are shown in the embodiments of Figs. 7-9.)

The paragraph beginning at line 22 on page 13 has been amended as follows:

Another implementation is described with reference to Figs. 6-7. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Fig. 6 is a sectional view or cut corresponding to that of Fig. 2, and depicts processing occurring subsequent to that of Fig. 2. Accordingly, an array 10b in accordance with this particular preferred embodiment is processed initially to the point as depicted in Fig. 2 in the first-described embodiment. A series of alternating trench isolation regions 22 and active areas 18 are thereby provided within semiconductor substrate 11 in a line adjacent and along at least a portion of lines of floating gates 12 and 14. Such defines a series of discrete transistor source areas separated by trench isolation regions. Floating gate word line patterning thereafter occurs, followed by drain region formation as described above. Lines of floating gates 12 and 14 as depicted in Fig. 7 (as well as in Figs. 8 and 9 described subsequently) comprise a gate dielectric layer, floating gate regions 23 formed thereover, an interpoly dielectric layer formed over floating gate regions 23, a conductively doped polysilicon/silicide stack formed over the interpoly dielectric layer, and an insulative cap (having an

outermost surface) formed over the conductively doped polysilicon/silicide stack.

The paragraph beginning at line 16 on page 15 has been amended as follows:

The photoresist is subsequently stripped, and an electrically insulative spacer forming layer is deposited over the entirety of the wafer. Such is ideally comprised of a different material than gate dielectric layer 43 of lines 12 and 14. Circuitry peripheral to the array is then preferably masked such that the entirety of the array remains open. Spacers for the lines of floating gates within the array, such as the depicted spacers 42 in Fig. 7 and having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface, are then formed by anisotropic etching to electrically isolate the sides of the lines of floating gates. Such preferably does not occur yet in the periphery which is why it is masked, as the preferred subsequently deposited polysilicon would otherwise result in polysilicon on monocrystalline silicon in the preferred embodiment over the peripheral transistor and other circuitry active areas. Unetched material 43 over drain locations 24 will separate monocrystalline silicon from polysilicon in this example embodiment. Alternately, if the peripheral gates are also initially formed such that the bottom gate dielectric layer is not etched and comprises a material different from the spacer layer, this material will separate polysilicon from monocrystalline silicon such that masking of the spacer forming layer in the periphery is immaterial.

In th Claims

Claim 54 is added.

END OF DOCUMENT

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